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# Greenbank Electronics

SC/MP Protoboard -2708.

Price £9-40 + 35p handling  
per order + 15% VAT

This board is substantially the same as the SC/MP Protoboard which it replaces.

The old board used to have a total of 1K EEPROM in two 5204's; the new board has circuitry to suit up to 2K of EEPROM in two 2708's.

Firmware which was previously offered in 5204's can now be made available in 2708's, at no extra charge for the larger memories. (Of course a 1/2K program in a 2708 will leave it half empty, let us know if this causes any problem in the specific system you are building - we will do our best to help.)

The necessity of the change has been brought about by the reduced prices for 2708's, which now makes them a considerably better buy than the 5204, and has effectively made the 5204 an unwise choice for new designs.

The only documentation we have on the new board is a new layout diagram, and the detailed hints and notes which were written for the earlier version.

If you require further information on the new board, or advice or assistance of any kind, please contact us again and we will let you know the latest situation.

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Kemitron SC/MP Protoboard from Greenbank

1. Introduction.

This versatile SC/MP based microprocessor board can be used in a number of ways;-

- i. as a stand-alone micro-computer,
- ii. as the processor card for a modular system,
- iii. as a prototyping system for micro-controlled applications.

These notes first explain how the dedicated parts of the board operate and then suggest various additions to the board.

2. Operation.

A system clock is using a quartz crystal together with C2, R5 and 6. A data bus connects the SC/MP chip to all the memory devices and is available adjacent to IC7 (DE $\phi$ -7) and at the edge connector. The address bus controls the location of the data in memory and decoding logic connected to this bus selects individual memory devices. Part of this address bus is available just below IC9 and the whole of it (AD $\phi$ -11) at the edge connector.

The read and write strobes (NRDS & NWDS) are combined to a composite strobe (NRWS) by half of IC3. NRWS is in turn combined with A11 and used to enable decoder IC5.b. This then decodes lines A9 & 1 $\phi$  so that ROM's (5204) -IC8 & 9, can be selected. IC8 is selected from address  $\phi\phi\phi$  to 1FF and IC9 can be located as required by patching to the appropriate decoder output. To do this join 'S' to 'S1, S2 or S3 ;-

S1.....2 $\phi\phi$  - 3FF .

S2.....4 $\phi\phi$  - 5FF

S3.....6 $\phi\phi$  - 7FF

Although when selecting ROM only the read strobe is needed, the use of  $\pi$  the composite strobe allows the use of these select lines also with RAM.

The RAM I/O chip is located so that RAM is available from F80 - FFF and the I/O ports use address space from F00 - F7F. This device is selected when address lines A8 - 11 are all high as detected by AND gate IC6. An additional chip select line (marked CS) is available which is active low. This may be needed in an expanded system to define the memory page (i.e. 4k block) in which the RAM I/O chip appears. Full details for using the RAM I/O are to be found in the manufacturers data sheet, but the following key addresses, valid for this board, may be helpful:-

F20.....Port A, data  
F21.....Port B, data  
F22.....Port A, output definition  
F23.....Port B, output definition  
F24.....Mode definition

The output ports are available as marked together with the power lines. It may be convenient to use 10 way plugs and sockets to connect to the ports (e.g. RS type 488-359).

The MPU and RAM I/O are initialised at power-on by the RC combination in conjunction with part of IC3. The system can also be reset at any time by using a reset switch connected from R to +5V.

The Flag lines F0-2, sense line A, Serial in (SIN) and out (SOUT) are all buffered and brought to the edge connector. The buffer IC-2 can drive miniature LED's directly via typically a 330R resistor.

### 3. Applications.

#### 1. Stand alone micro-computer.

The board can be used together with a teletype-like device and the National KITBUG software. To do this the KITBUG ROM should be inserted as IC8. The RAM I/O chip provides the necessary scratch pad memory for KITBUG and some left for holding programs or data. In this mode flag bit 0 should be buffered and inverted using part of IC3 and used as the output and sense line B should be buffered and used as input. The input and output then use the convention that the rest state is a high level and a start bit is a low level.

The board is also suitable for use as the basis of a direct memory addressed VDU system, either with a serial or parallel keyboard input. Suitable software is available.

ii. Processor card.

All the data and address lines are available at the edge connector together with the read and write control strobes. These lines can be extended across to other cards to provide additional RAM, ROM or peripheral interfaces. The SC/MP chip provides adequate drive current for up to 4k ROM's and 4k RAM, but buffering may be required for larger systems.

iii. As a micro-controller.

The RAM I/O chip provides 16 I/O lines and a further 7 are available on the SC/MP chip. These can be used to sense external conditions and to control other devices. This wealth of I/O lines makes this card very suitable for control applications. Additional flexibility is provided by the extensive patch areas to allow extra devices to be added as required. Some suggestions for interfacing displays, keyboards etc are sketched out in the next section.

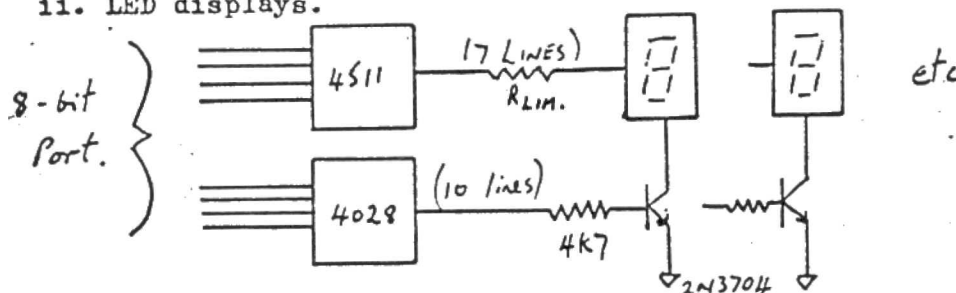
#### 4. Hang-ons.

##### i. Extra memory.

Use pairs of 2112 devices to add memory in blocks of 256 bytes. IC5.a is a spare decoder and can be used to select these.

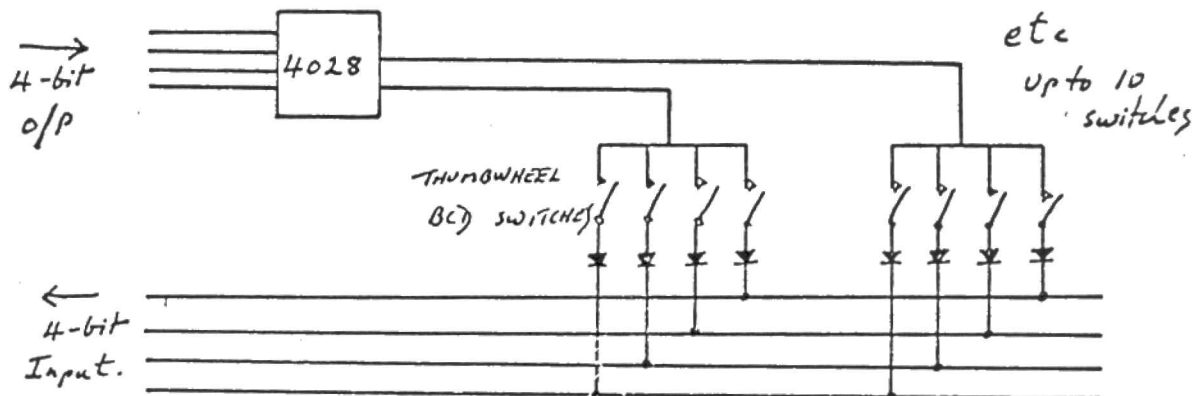
Use pairs of 2114 devices to add memory in blocks of 1k.

##### ii. LED displays.



To drive only 4 digits or less the BCD decoder (4028) can be omitted and the transistors driven directly by the port. For direct drive pull-up resistors should be added. By either using a 74154 or two 4028's up to 16 digits can be driven from a single port. With larger displays more segment drive current may be required than is available from the 4511. Rich people may prefer the 74C912 (BCD) or 74C917 (Hex) as complete display controllers.

##### iii. BCD input.



##### iv. Keyboards.

Arrange switches in a matrix (say 4x4) and strobe rows with one set of lines and sense the columns with another set. Alternatively latch the column data and change the output definition of the port and use the same lines as strobes and sense.

Rich people may like to try 74C922 (16 keys) or 74C923 (20 keys) as complete keyboard scanner-encoders.

v. More I/O

More inputs can be added using tri-state buffers connected to the data bus e.g. 4503 for 6-bits and 81LS95 for 8-bits. Address lines should be decoded ( 74LS138,139 or 8131) and used to enable the buffers at the appropriate address.

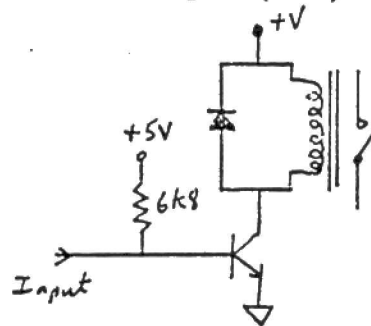
Latched outputs can be provided using 4042's (4-bit) and latched I/O using 74C373.(8-bit).

vi. Serial I/O.

SC/MP provides for both serial input (SIN) and output (SOUT).

vii. Driving relays.

Don't forget the  
catching diode \*\*\*



ix. Mains loads.

Either isolate using a realy as above or use an opto-isolator controlling a triac (see RS application note R/2129).

JSD

7.9.78

Date 30/7/78

# COMPONENTS

R1 10K  
2 1K  
3 4K7  
4 10K  
5 10K  
6 100K  
7 1K  
8 10K  
9 10K

C1 100µ, 10V  
2 47µ, 10V  
3 47 pF  
4 0.1µ DISC  
5 0.1µ DISC

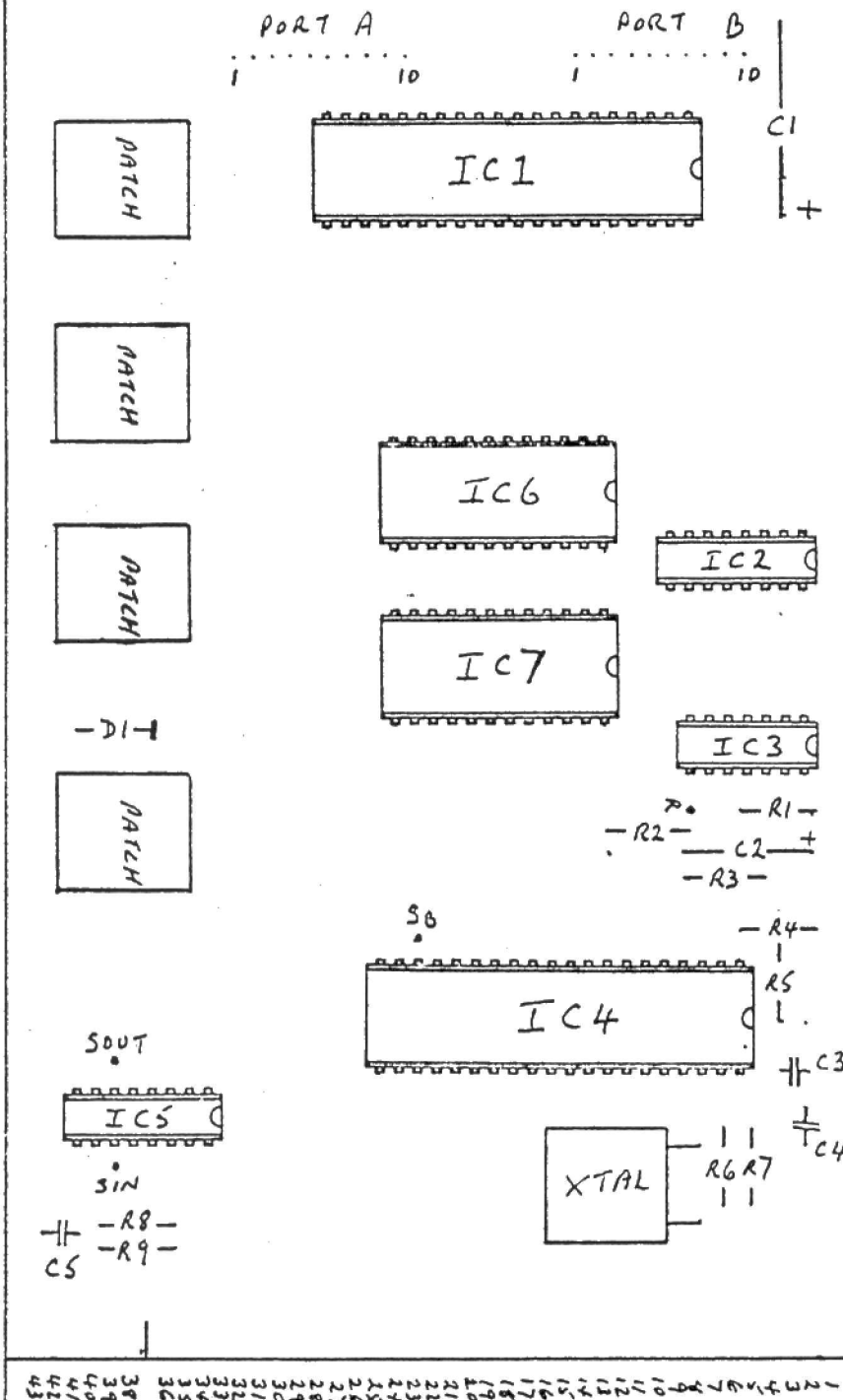
IC1 INS 8154  
2 74LS139  
3 74LS132  
4 INS 8060  
5 4050  
(6 2708 )  
(7 2708 )

(D1 6V8 ZENER )

D1 IS ONLY FITTED  
WHEN THE SYSTEM IS USING  
A -12V SUPPLY.  
RESET SWITCH R TO +5V.  
XTAL 2 OR 4MHZ

PORT A PIN 1 +5V  
2 PA0  
3 PA1  
4 PA2  
5 PA3  
6 GND  
7 PA4  
8 PA5  
9 PA6  
10 PA7

PORT B PIN 1 PB0  
2 PB1  
3 PB2  
4 PB3  
5 PB4  
6 PB5  
7 PB6  
8 PB7  
9 +5V  
10 GND



Kemitron Electronics

2708 VERSION

SC-MP-2

Drn. J.S.D

Date 12/11/79